UNIFIED DIGITAL ARCHITECTURE

ABSTRACT OF THE DISCLOSURE

A unified, unidirectional serial link is described for providing data across wired media, such as a chip-to chip or a card-to-card interconnect. It consists of a transmit section and a receive section that are operated as pairs to allow the serial data communication. The serial link is implemented as part of a VLSI ASIC module and derives its power, data and clocking requirements from the host modules. The logic transmitter portion contains a phase locked loop (PLL) , a dibit data register, a finite impulse response (FIR) filter and a transmit data register. The phase locked loop comprises both a digital coarse loop and an analog fine loop. The digital receiver portion contains a PLL, an FIR phase rotator, a phase rotator control state machine, and a clock buffer. The transmitter and the receiver each preferably utilize a pseudo-random bit stream (PRBS) generator and checker.